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Renesas Electronics website: <http://www.renesas.com>

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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SWITCHING

N-CHANNEL POWER MOSFET

DESCRIPTION

The NP88N04NUG is N-channel MOS Field Effect Transistor designed for high current switching applications.

ORDERING INFORMATION

PART NUMBER	PACKAGE
NP88N04NUG	TO-262

FEATURES

- Channel temperature 175 degree rating
- Super low on-state resistance
 $R_{DS(on)} = 3.4 \text{ m}\Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 44 \text{ A)}$
- Low C_{iss} : $C_{iss} = 9510 \text{ pF TYP. (} V_{DS} = 25 \text{ V)}$

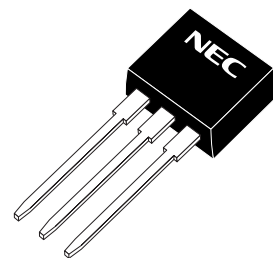
(TO-262)

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$)

Drain to Source Voltage ($V_{GS} = 0 \text{ V}$)	V_{DSS}	40	V
Gate to Source Voltage ($V_{DS} = 0 \text{ V}$)	V_{GSS}	± 20	V
Drain Current (DC) ($T_C = 25^\circ\text{C}$)	$I_{D(DC)}$	± 88	A
Drain Current (pulse) ^{Note1}	$I_{D(pulse)}$	± 352	A
Total Power Dissipation	P_{T1}	1.8	W
Total Power Dissipation ($T_C = 25^\circ\text{C}$)	P_{T2}	200	W
Channel Temperature	T_{ch}	175	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +175	$^\circ\text{C}$
Repetitive Avalanche Current ^{Note2}	I_{AR}	56	A
Repetitive Avalanche Energy ^{Note2}	E_{AR}	314	mJ

Notes 1. $PW \leq 10 \mu\text{s}$, Duty Cycle $\leq 1\%$

2. $T_{ch} \leq 150^\circ\text{C}$, $V_{DD} = 20 \text{ V}$, $R_G = 25 \Omega$, $V_{GS} = 20 \rightarrow 0 \text{ V}$



THERMAL RESISTANCE

Channel to Case Thermal Resistance	$R_{th(ch-C)}$	0.75	$^\circ\text{C/W}$
Channel to Ambient Thermal Resistance	$R_{th(ch-A)}$	83.3	$^\circ\text{C/W}$

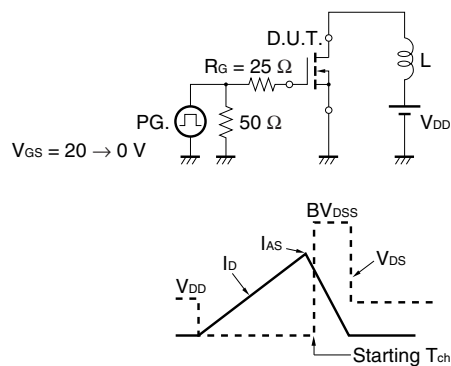
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ELECTRICAL CHARACTERISTICS (T_A = 25°C)

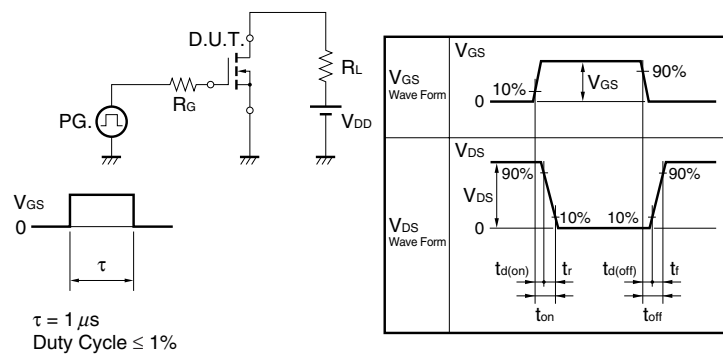
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 40 V, V _{GS} = 0 V			1	μA
Gate Leakage Current	I _{GSS}	V _{GS} = ±20 V, V _{DS} = 0 V			±100	nA
Gate to Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	2.0	3.0	4.0	V
Forward Transfer Admittance ^{Note}	y _{fs}	V _{DS} = 10 V, I _D = 44 A	27	51		S
Drain to Source On-state Resistance ^{Note}	R _{DS(on)}	V _{GS} = 10 V, I _D = 44 A		2.6	3.4	mΩ
Input Capacitance	C _{iss}	V _{DS} = 25 V		9510	15000	pF
Output Capacitance	C _{oss}	V _{GS} = 0 V		880	1370	pF
Reverse Transfer Capacitance	C _{rss}	f = 1 MHz		570	990	pF
Turn-on Delay Time	t _{d(on)}	V _{DD} = 20 V, I _D = 44 A		43	100	ns
Rise Time	t _r	V _{GS} = 10 V		104	260	ns
Turn-off Delay Time	t _{d(off)}	R _G = 0 Ω		107	220	ns
Fall Time	t _f			22	60	ns
Total Gate Charge	Q _G	V _{DD} = 32 V		171	250	nC
Gate to Source Charge	Q _{GS}	V _{GS} = 10 V		38		nC
Gate to Drain Charge	Q _{GD}	I _D = 88 A		58		nC
Body Diode Forward Voltage ^{Note}	V _{F(S-D)}	I _F = 88 A, V _{GS} = 0 V	0.94	1.5		V
Reverse Recovery Time	t _{rr}	I _F = 88 A, V _{GS} = 0 V		51		ns
Reverse Recovery Charge	Q _{rr}	di/dt = 100 A/μs		67		nC

Note Pulsed

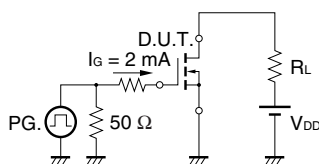
TEST CIRCUIT 1 AVALANCHE CAPABILITY



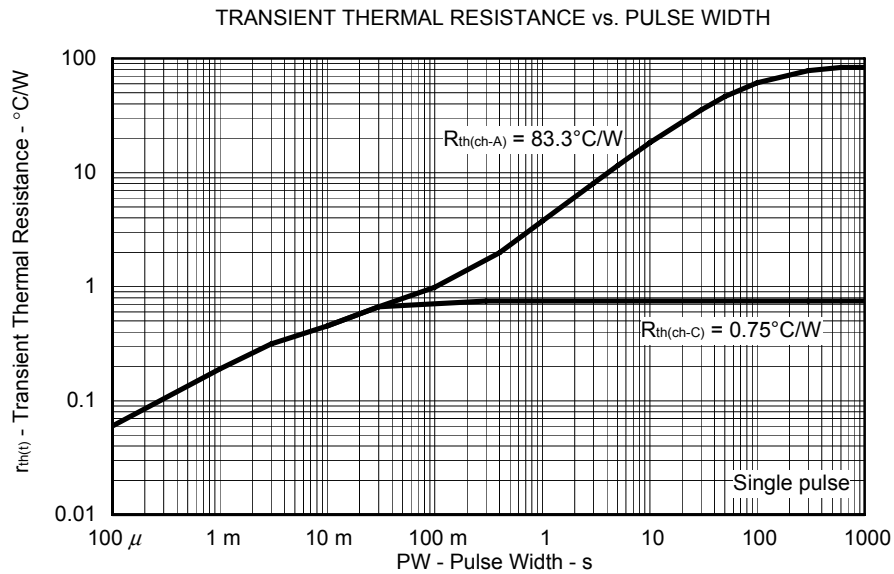
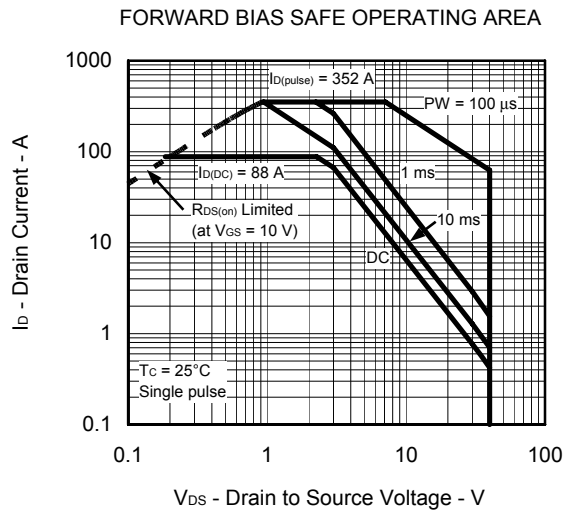
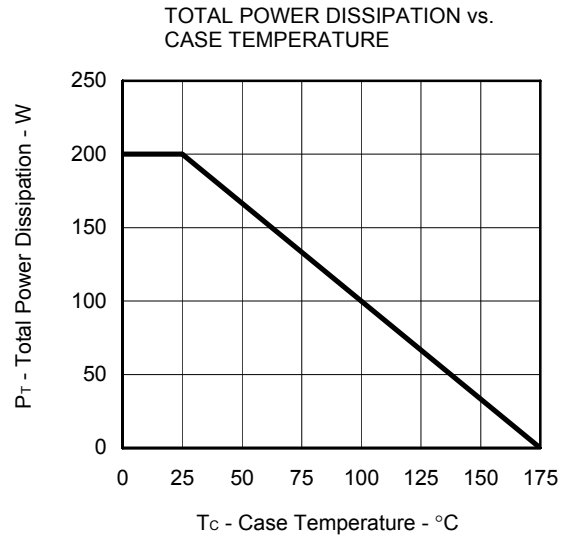
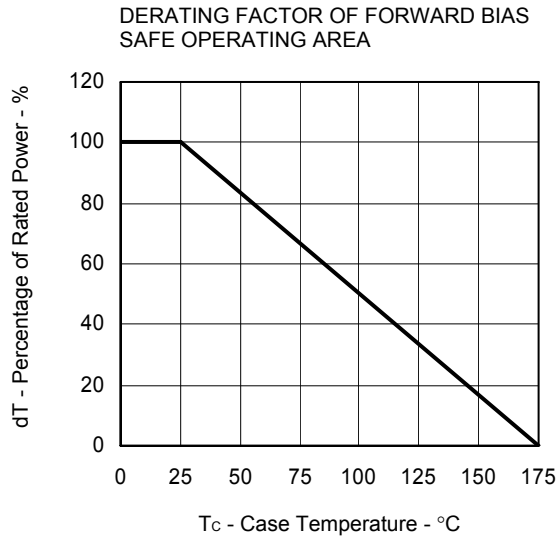
TEST CIRCUIT 2 SWITCHING TIME



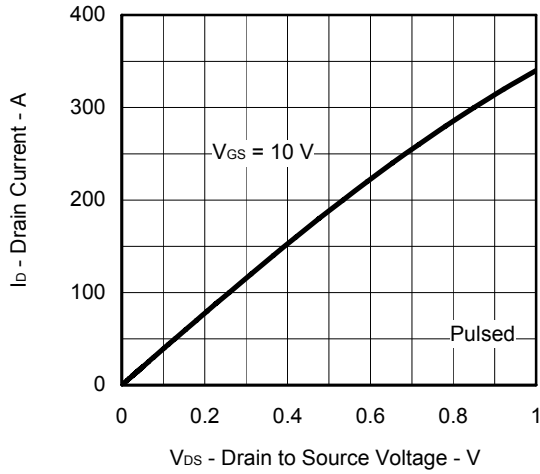
TEST CIRCUIT 3 GATE CHARGE



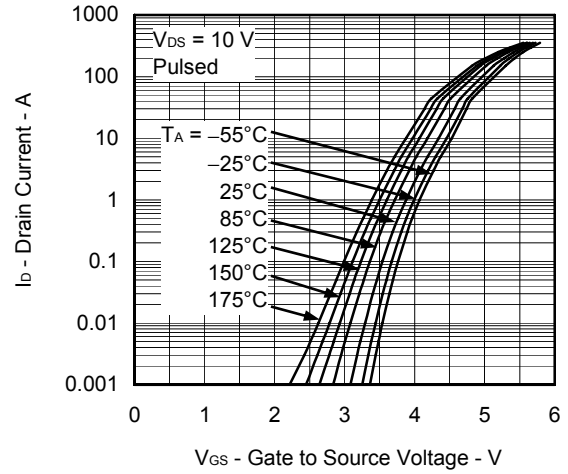
TYPICAL CHARACTERISTICS (T_A = 25°C)



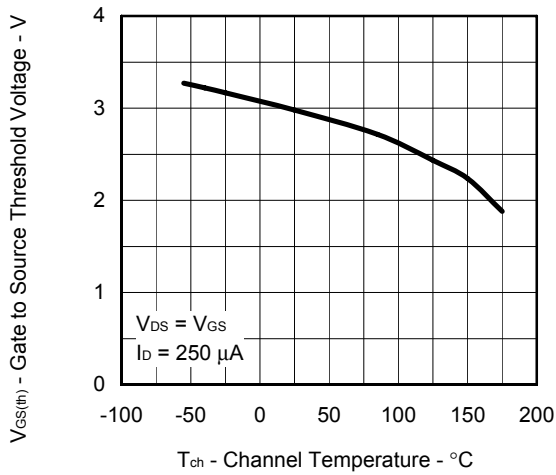
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



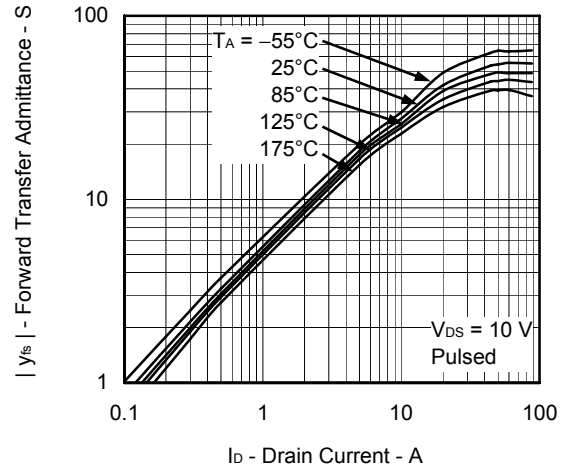
FORWARD TRANSFER CHARACTERISTICS



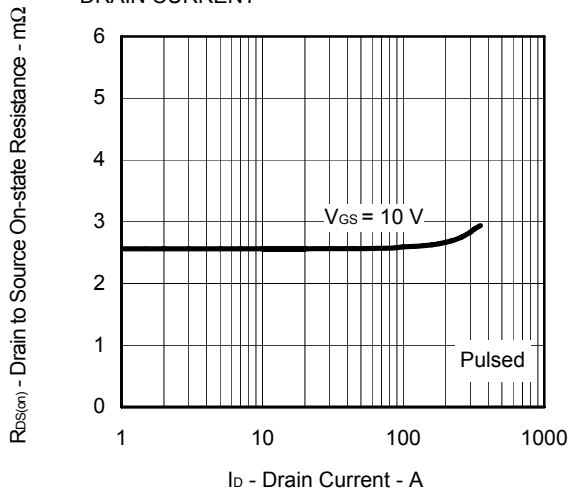
GATE TO SOURCE THRESHOLD VOLTAGE vs. CHANNEL TEMPERATURE



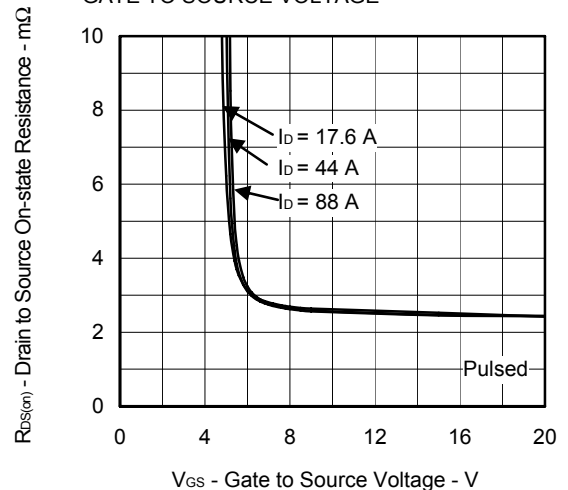
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



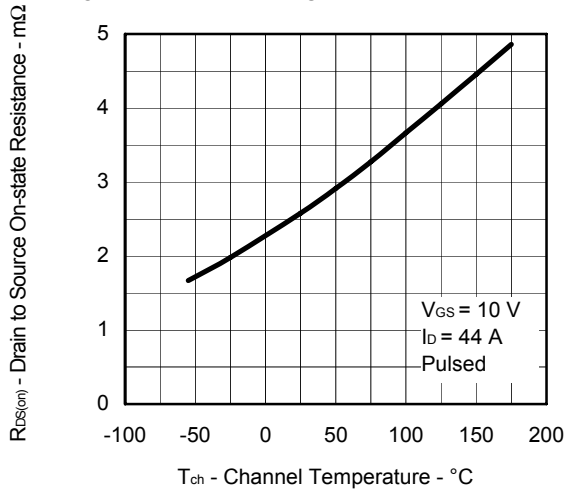
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



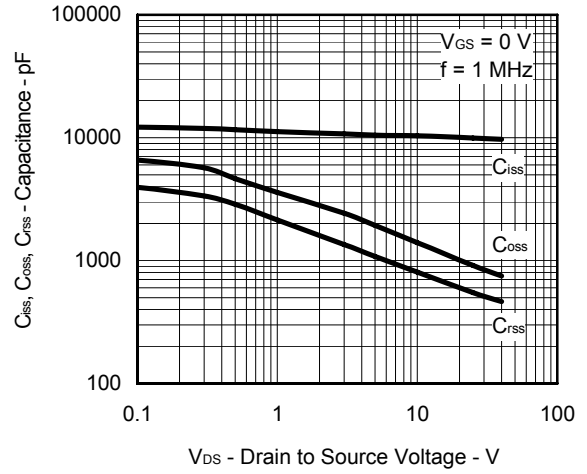
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



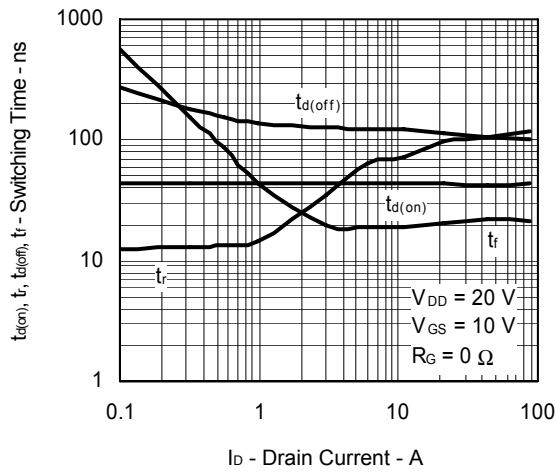
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



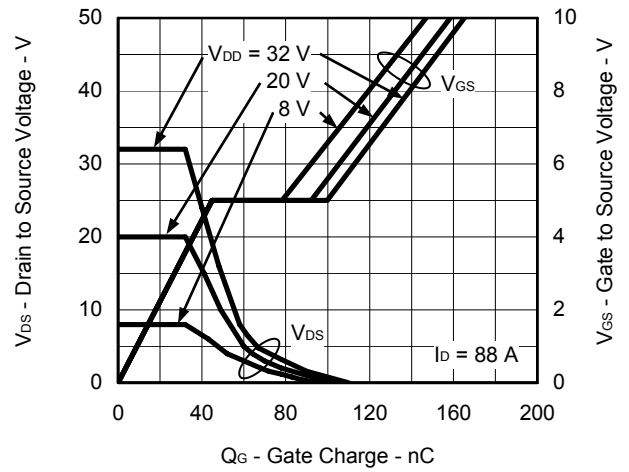
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



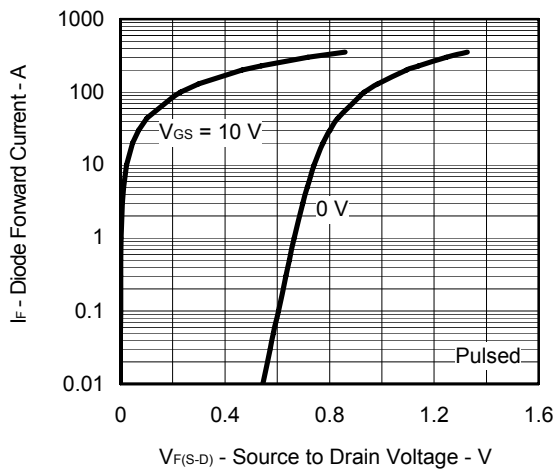
SWITCHING CHARACTERISTICS



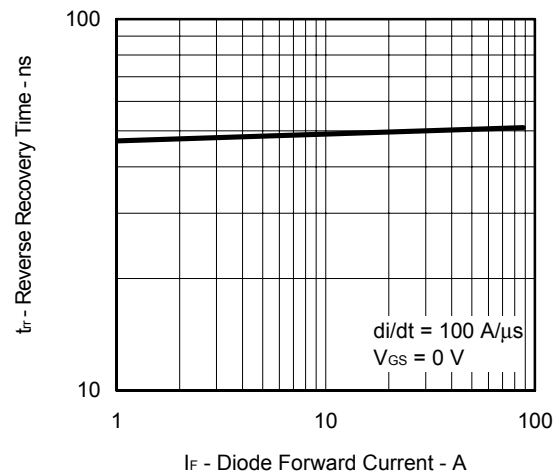
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE

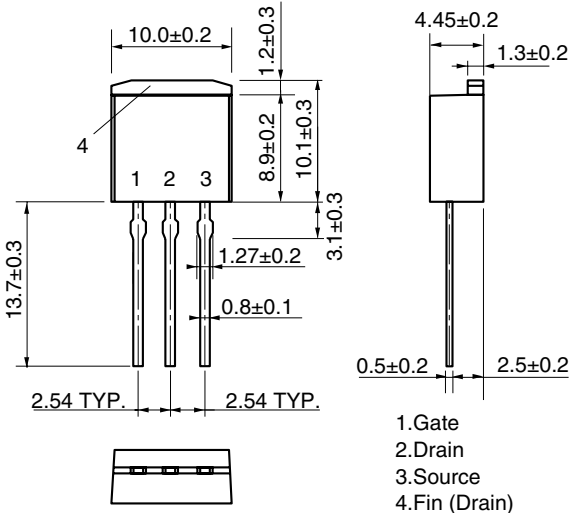


REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT

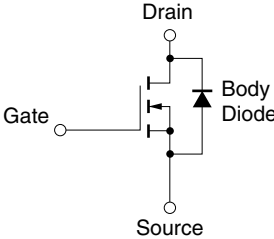


PACKAGE DRAWING (Unit: mm)

TO-262 (Revised)



EQUIVALENT CIRCUIT



Remark Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

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